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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,881	WILKERSON, CHRISTOPHER B.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-11 and 31-34* is/are allowed.

6)☒ Claim(s) *1,3,6,7,12,14,17-19,21,24-26,28 and 35-38* is/are rejected.

7)☒ Claim(s) *2,4,5,13,15,16,20,22,23,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 35-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 35, line 4 states "bypassing execution of instructions...", however line 7, states "re-executing bypassed instructions...". It is unclear how a bypassed instruction is re-executed. How can an instruction that never gets executed get re-executed? For the purposes of examination, the claimed bypassing and re-executing limitations will be interpreted as pausing the execution of an instruction until at least one instruction results in a cache miss and executing the bypassed instructions once the cache is loaded with cache miss data. Appropriate correction is required.

4. Claims 36-38 are rejected for incorporating the defects of claim 35.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 6, 7, 19, 21, 24, 25, 26, and 28 are rejected under 35 U.S.C. 102 (b) as being anticipated by Yoaz et al., US Patent 5,987,595 (hereinafter referred to as Yoaz).

7. Referring to claim 1, Yoaz have taught a method comprising:

a. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 35-67, column 5, lines 40-50, The system executes instructions out of order which is speculative. During this speculative execution, potential operand collisions are identified.); and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (Figure 5, column 5, line 40-column 6, line 50, column 6, line 61-column 7, line 24, Status bits, including operand dependency bits, are set in the reorder buffer for colliding and potentially colliding instructions.);

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (abstract, column 3, lines 35-67, column 5, lines 40-50, Colliding and potentially colliding instructions are bypassed until the instructions from which they depend actually execute.).

8. Referring to claim 3, Yoaz have taught the method of claim 1, as described above, and further comprising: propagating the tag to destination registers of the instructions to indicate that an operand within the destination registers is a scratch value (column 6, line 31-column 7, line 25, When operand destination registers in instructions are detected as colliding or potentially colliding, then dependency bits of load and store instructions are set.).

9. Referring to claim 6, Yoaz have taught the method of claim 1 as described above, and further comprising: marking each instruction in a pipeline with a tag to indicate if the instruction involves a scratch value (Figure 5, Instructions are marked with status bits in the reorder buffer.).

10. Referring to claim 7, Yoaz have taught the method of claim 1 as described above, and further comprising: propagating the tag through a store buffer if an address generation register does not indicate that the address generation register holds a scratch value (Figure 5, Tags of store instructions are propagated through the reorder buffer until retirement.).

11. Referring to claim 19, Yoaz have taught a system comprising:

a. a memory, a storage device, and a processor each coupled to a bus (Figure 3);

b. the processor including an execution engine having instructions which when executed by the processor cause the processor to perform actions including:

i. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 35-67, column 5, lines 40-50, The system executes instructions out of order which is speculative. During this speculative execution, potential operand collisions are identified.);

ii. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (Figure 5, column 5, line 40-column 6, line 50, column 6, line 61-column 7, line 24, Status bits, including operand dependency bits, are set in the reorder buffer for colliding and potentially colliding instructions.); and

iii. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (abstract, column

3, lines 35-67, column 5, lines 40-50, Colliding and potentially colliding instructions are bypassed until the instructions from which they depend actually execute.).

12. Claims 21, 24, and 25 do not recite limitations above the claimed invention set forth in claims 3, 6, and 7, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 3, 6, and 7 above.

13. Claims 26 and 28 do not recite limitations above the claimed invention set forth in claims 1 and 3, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 1 and 3 above.

14. Claims 35-38 are rejected under 35 U.S.C. 102 (b) as being anticipated by Parady, US Patent 5,933,627.

15. Referring to claim 35, Parady have taught a method comprising:

a. setting a tag of a register when an instruction having the register as a destination results in a cache miss, to identify the register as containing a scratch value (Figure 2, element 80);

b. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value until at least one instruction is detected that results in a cache miss (abstract, Thread 0 is bypassed when Thread 3 is executing until thread 3 experiences a cache miss.); and

c. re-executing bypassed instructions once a cache is loaded with cache miss data (abstract, Figure 3, column 3, line 35-column 4, line 64, The threads are switched in a round

robin fashion. Thread 0 is reexecuted each time after threads 1, 2, and 3 finish executing. Thread 0 is reexecuted many times after the cache is loaded with the miss data.).

16. Referring to claim 36, Parady has taught the method of claim 35, as described above, and further comprising:

a. executing store instructions having a tag to indicate that the instruction involves a scratch value if tag values associated with operands of the store instruction indicate non-scratch values (Figure 2, column 3, lines 25-35, Instructions with valid tags are executed.).

17. Referring to claim 37, Parady has taught the method of claim 35, as described above, and further comprising:

a. propagating the tag to destination registers of the instructions to indicate that an operand within the destination registers is a scratch value (Figure 2, The tags are constantly maintained, and as such are propagated to the destination registers at all times.).

18. Referring to claim 38, Parady has taught the method of claim 35, as described above, and further comprising:

a. servicing detected cache miss instructions in parallel prior to re-executing the bypassed instructions (column 4, lines 41-52).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 12, 14, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al., US Patent 5,651,125 (herein after referred to as Witt et al.), in view of Yoaz, US Patent 5,987,595 (herein after referred to as Yoaz).

21. Referring to claim 12, Witt et al. have taught a processor comprising:

a. at least two arithmetic units (Figure 6B, 840R, 845R);

b. a translation look aside buffer (Figure 6B, 915);

c. a branch prediction unit (Figure 6A, element 825); and

22. Witt et al. have not taught an execution engine having a plurality of instructions which when executed cause the processor to perform actions including:

a. identifying scratch values generated during speculative execution of a processor, and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value.

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value.

23. However, Yoaz have taught ~~taught~~ an execution engine having a plurality of instructions which when executed cause the processor to perform actions including:

a. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 35-67, column 5, lines 40-50, The system executes instructions out of order which is speculative. During this speculative execution, potential operand collisions are identified.), and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (Figure 5, column 5, line 40-column 6, line 50, column 6, line 61-column 7, line 24, Status bits, including operand dependency bits, are set in the reorder buffer for colliding and potentially colliding instructions.), for the desirable purpose of predicting colliding instructions to avoid costly flushes, while still allowing the advancement of other instructions (column 2, lines 25-29).

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (abstract, column 3, lines 35-67, column 5, lines 40-50, Colliding and potentially colliding instructions are bypassed until the instructions from which they depend actually execute.)

24. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Witt et al. include the claimed execution engine and instructions, as taught by Yoaz, for the desirable purpose of for the desirable purpose of predicting colliding instructions to avoid costly flushes, while still allowing the advancement of other instructions (column 2, lines 25-29).

25. Claims 14, 17, and 18 do not recite limitations above the claimed invention set forth in claims 3, 6, and 7 are respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 3, 6, and 7 above.

Allowable Subject Matter

26. Claims 8-11 and 31-34 are allowed.

27. Claims 2, 4, 5, 13, 15, 16, 20, 22, 23, 27, 29, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

28. Applicant's arguments with respect to claims 1, 3, 6, 7, 12, 14, 17, 18, 19, 21, 24, 25, 26, 28, and 35-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

1/20/06

HENRY W. H. TSAI
PRIMARY EXAMINER